IN THE CLAIMS:

Please cancel claims 16 through 63 without prejudice or disclaimer to pursuit of the subject matter thereof in a continuing application.

Claims 1 through 15 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently amended) A method for manufacturing an interconnect structure ~~comprising~~ consisting essentially of:

forming a recess within a dielectric material situated on a semiconductor ~~lower~~ substrate, ~~said~~ the recess extending below a top surface of ~~said~~ the dielectric material;

forming a diffusion barrier layer substantially conformally on the top surface of the dielectric material and over an interior surface of the recess ~~within the dielectric material~~;

forming a seed layer on the diffusion barrier layer over the top surface of the dielectric material and within the recess, the diffusion barrier layer ~~being composed of~~ comprising a material having a melting point greater than or equal to that of a material ~~from which~~ comprising the seed layer ~~is composed~~;

forming an electrically conductive layer on the seed layer ~~including the portion of the seed layer~~ over the top surface of the dielectric material and within ~~said~~ the recess, the material ~~from which~~ comprising the diffusion barrier layer ~~is composed~~ having a melting point greater than that of a material ~~from which~~ comprising the electrically conductive layer ~~is composed~~, the material ~~from which~~ comprising the seed layer ~~is composed~~ having a melting point greater than or equal to that of the material ~~from which~~ comprising the electrically conductive layer ~~is composed~~;

forming an energy absorbing layer on ~~said~~ the electrically conductive layer, ~~said~~ the energy absorbing layer having a greater thermal absorption capacity than that of ~~said~~ the electrically conductive layer;

applying, omnidirectionally, energy to ~~said~~ the energy absorbing layer sufficient to cause ~~said~~ the electrically conductive layer to flow within ~~said~~ the recess; and

removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

2. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein forming a diffusion barrier layer on the recess within the dielectric material ~~is a~~ is effected by CVD ~~deposition step~~.

3. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material ~~from which~~ comprising the diffusion barrier layer ~~is composed~~ is selected from the group consisting of ceramics, metallics, and intermetallics.

4. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material ~~from which~~ comprising the diffusion barrier layer ~~is composed~~ is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

5. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, further comprising, prior to forming a seed layer on the diffusion barrier layer, heating the diffusion barrier layer ~~is an~~ in an environment substantially containing a nitrogen gas.

6. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein depositing a seed layer on the diffusion barrier layer ~~is a~~ is effected by CVD ~~deposition step~~.

7. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material ~~from which~~ comprising the seed layer ~~is composed~~ is selected from the group consisting of ceramics, metallics, and intermetallics.

8. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material ~~from which~~ comprising the seed layer ~~is composed~~ is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

9. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material ~~from which~~ comprising the electrically conductive layer ~~is composed~~ is selected from the group consisting of aluminum and copper.

10. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the energy absorbing layer ~~is composed of~~ comprises a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

11. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein applying energy to ~~said~~ the energy absorbing layer utilizes a furnace.

12. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein removing portions of the energy absorbing layer and the electrically conductive layer ~~is an~~ comprises abrasive planarization ~~step~~.

13. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 12, wherein removing portions of the energy absorbing layer and the electrically conductive layer ~~is a~~ comprises chemical mechanical ~~planarizing step~~ planarization.

14. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, ~~wherein~~ further comprising forming the recess ~~has~~ to have an aspect ratio greater than about four (4) to one (1).

15. (Currently amended) A method for manufacturing an interconnect structure as recited in Claim 1, ~~wherein~~ further comprising forming the recess ~~comprises~~ to comprise a contact hole situated below a trench, ~~said semiconductor substrate assembly having a lower substrate defining a plane, said~~ the contact hole terminating at an end thereof at ~~said lower~~ the semiconductor substrate and terminating at an opposite end thereof at ~~said~~ the trench, ~~said~~ the trench extending from ~~said~~ the opposite end of ~~said~~ the contact hole ~~to a~~ to the top surface of ~~said~~ the dielectric material, the trench extending parallel to the plane of the ~~lower~~ semiconductor substrate.

Claims 16 through 63 (Canceled).